WHAT IS CLAIMED IS:

1. A gain voltage controller for use with a sampled grating distributed Bragg reflector (SGDBR) laser, comprising:

a controller for providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

a voltage monitor coupled to a gain section of the laser for monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

wherein the controller controls the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

2. The gain voltage controller of claim 1, wherein the controller keeps the front mirror controlled by the front mirror current and the back mirror controlled by the back mirror current aligned with a cavity mode of the laser.

3. The gain voltage controller of claim 1, wherein the controller comprises a digital signal processor (DSP) to control the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

4. The gain voltage controller of claim 3, wherein the DSP dithers the front and back mirror currents.

5. The gain voltage controller of claim 3, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

6. The gain voltage controller of claim 5, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

7. The gain voltage controller of claim 6, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

8. The gain voltage controller of claim 7, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

9. The gain voltage controller of claim 3, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

10. The gain voltage controller of claim 9, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

11. The gain voltage controller of claim 9, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

12. The gain voltage controller of claim 9, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

13. The gain voltage controller of claim 9, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

14. The gain voltage controller of claim 13, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

15. The gain voltage controller of claim 13, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

16. The gain voltage controller of claim 13, wherein the gradient descent adaptation algorithm is an LMS algorithm.

17. The gain voltage controller of claim 13, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

18. The gain voltage controller of claim 9, wherein the LMS estimator is achieved using an adaptive linear filter.

19. The gain voltage controller of claim 9, wherein the LMS estimator is driven by white noise.

20. The gain voltage controller of claim 9, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

21. The gain voltage controller of claim 9, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

22. The gain voltage controller of claim 1, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

23. The gain voltage controller of claim 22, wherein the analog circuit comprises at least one phase locker circuit.

24. The gain voltage controller of claim 23, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

25. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses a phase lock loop.

26. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses an RF dither locker.

27. The gain voltage controller of claim 23, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

28. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

29. The gain voltage controller of claim 28, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

30. The gain voltage controller of claim 28, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

31. The gain voltage controller of claim 28, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

32. The gain voltage controller of claim 28, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

33. The gain voltage controller of claim 28, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

34. The gain voltage controller of claim 28, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

35. The gain voltage controller of claim 1, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.

36. A method of controlling a sampled grating distributed Bragg reflector (SGDBR) laser, comprising the steps of:

providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

controlling the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

37. The method of claim 36, wherein the front mirror is controlled by the front mirror current and the back mirror is controlled by the back mirror current aligned with a cavity mode of the laser.

38. The method of claim 36, wherein a digital signal processor (DSP) controls the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

39. The method of claim 38, wherein the DSP dithers the front and back mirror currents.

40. The method of claim 38, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

41. The method of claim 40, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

42. The method of claim 41, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

43. The method of claim 42, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

44. The method of claim 38, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

45. The method of claim 44, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

46. The method of claim 44, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

47. The method of claim 44, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

48. The method of claim 44, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

49. The method of claim 48, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

50. The method of claim 48, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

51. The method of claim 48, wherein the gradient descent adaptation algorithm is an LMS algorithm.

52. The method of claim 48, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

53. The method of claim 44, wherein the LMS estimator is achieved using an adaptive linear filter.

54. The method of claim 44, wherein the LMS estimator is driven by white noise.

55. The method of claim 44, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

56. The method of claim 44, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

57. The method of claim 36, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

58. The method of claim 57, wherein the analog circuit comprises at least one phase locker circuit.

59. The method of claim 58, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

60. The method of claim 58, wherein the at least one phase locker circuit uses a phase lock loop.

61. The method of claim 58, wherein the at least one phase locker circuit uses an RF dither locker.

62. The method of claim 58, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

63. The method of claim 58, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

64. The method of claim 63, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

65. The method of claim 63, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

66. The method of claim 63, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

67. The method of claim 63, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

68. The method of claim 63, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

69. The method of claim 63, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

70. The method of claim 36, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.

71. An article of manufacture embodying logic to implement a method of controlling a sampled grating distributed Bragg reflector (SGDBR) laser, comprising the steps of:

providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

controlling the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

72. The article of claim 71, wherein the front mirror is controlled by the front mirror current and the back mirror is controlled by the back mirror current aligned with a cavity mode of the laser.

73. The article of claim 71, wherein a digital signal processor (DSP) controls the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

74. The article of claim 73, wherein the DSP dithers the front and back mirror currents.

75. The article of claim 73, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

76. The article of claim 75, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

77. The article of claim 76, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

78. The article of claim 77, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

79. The article of claim 73, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

80. The article of claim 79, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

81. The article of claim 79, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

82. The article of claim 79, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

83. The article of claim 79, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

84. The article of claim 83, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

85. The article of claim 83, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

86. The article of claim 83, wherein the gradient descent adaptation algorithm is an LMS algorithm.

87. The article of claim 83, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

88. The article of claim 83, wherein the LMS estimator is achieved using an adaptive linear filter.

89. The article of claim 83, wherein the LMS estimator is driven by white noise.

90. The article of claim 83, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

91. The article of claim 83, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

92. The article of claim 71, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

93. The article of claim 92, wherein the analog circuit comprises at least one phase locker circuit.

94. The article of claim 93, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

95. The article of claim 93, wherein the at least one phase locker circuit uses a phase lock loop.

96. The article of claim 93, wherein the at least one phase locker circuit uses an RF dither locker.

97. The article of claim 93, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

98. The article of claim 93, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

99. The article of claim 98, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

100. The article of claim 98, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

101. The article of claim 98, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

102. The article of claim 98, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

103. The article of claim 98, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

104. The article of claim 98, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

105. The article of claim 71, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.